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CENTRAL FAX CENTER Application Serial No.: 10/670,219  
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REMARKS

The Official Action dated October 6, 2006 has been received and its contents carefully noted. In view thereof claims 1, 21 and 26 have been amended in order to better define that which Applicant regards as the invention. As previously, claims 1-29 are presently pending in the instant application with claims 6-20 being withdrawn from further consideration by the Examiner as being directed to a non-elected invention.

With reference to the Official Action and particularly page 2 thereof, Applicant again confirms the election of claims 1-5 and 21-29 for prosecution on the merits, this election being made without traverse on February 11, 2005.

Turning now to page 3 of the Office Action, the disclosure has been objected to as including a minor informality, as can be seen from the foregoing, the specification at page 8 has been amended to properly refer to Fig. 2 rather than Fig. 3. Accordingly, it is respectfully submitted that Applicant's specification as presently amended is now in proper formal condition for allowance.

Further on page 2 of the Office Action, claims 1, 21 and 26 have been rejected under 35 U.S.C. §112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Particularly, the Examiner notes with regard to claim 1 that it is not clear whether a "predetermined voltage being supplied to a predetermined terminal" in lines 6 and 7 is referring to "a signal inputted to the predetermined terminal" in line 8. For the purposes of examination, the Examiner assumed that "a predetermined voltage" in lines 6 and 7 is that of "a signal" in line 8. As can be seen from the foregoing amendments, independent claim 1 has been amended to recite a test mode circuit for outputting a test mode signal according to a predetermined voltage to a predetermined terminal of the plurality of address input terminals when a signal is inputted to

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the predetermined terminal or the plurality of address input terminals. In this regard, it is confirmed that the Examiner's understanding with respect to independent claim 1 is correct.

With respect to independent claims 21 and 26, these claims have likewise been amended in order to clarify that which is set forth by Applicant's claimed invention and confirms the Examiner's understanding in this regard. Accordingly, it is respectfully submitted that each of independent claims 1, 21 and 26 as well as those claims which depend therefrom are now in proper formal condition for allowance.

Turning now to paragraph 8 of the Office Action, claims 1, 3-5, 21, 23-26, 28 and 29 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Admitted Prior Art ("Admission") in view of U.S. Patent No. 6,112,322 issued to McGibney et al. and U.S. Patent No. 6,037,792 issued to McClure. This rejection is respectfully traversed in that the combination proposed by the Examiner neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

In this regard, as can be seen from the foregoing amendments to independent claim 1 as well as similar amendments carried out with respect to independent claims 21 and 26, Applicant's claimed invention now recites a nonvolatile semiconductor memory device comprising a memory cell array having a plurality of memory cells and arranged in an array, the cells being connected to a plurality of bit lines and word lines, a plurality of address input terminals inputting a plurality of addresses thereto, a test mode circuit for outputting a test mode signal according to a predetermined voltage to a predetermined terminal of the plurality of address input terminals when a signal is inputted to the predetermined terminal among the plurality of address input terminals, a row decoder connected to the test mode circuit and applying an excess voltage for a test to all the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and setting all the bit lines to a non-selecting state

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in response to the test mode signal and a monitor terminal connected to the test mode circuit and outputting the test mode signal for confirming a test mode. That is, in accordance with the present invention, the nonvolatile semiconductor memory device includes a test mode circuit and a monitor terminal. The test mode circuit outputs a test mode signal according to a predetermined voltage to a predetermined terminal in a plurality of address input terminals. The monitor terminal is connected to the test mode circuit for receiving the test mode signal for confirming a test mode of the memory device from the outside. The nonvolatile semiconductor memory device according to the present invention achieves the advantages set forth in accordance with Applicant's specification.

In rejecting Applicant's claimed invention, the Examiner states that Applicant's Admission includes a test mode circuit for outputting a test mode signal according to a predetermined voltage being supplied to a predetermined terminal when a signal is inputted to the predetermined terminal. The Examiner states that it is implied from the Admissions that the test mode circuit is provided for controlling the operations of columns. Further, the Examiner is of the position that a signal from the exterior implies that the test mode circuit for outputting the test mode circuit according to a predetermined voltage being supplied to a predetermined terminal when the signal is inputted to the predetermined terminal is likewise shown by Applicant's Admissions, however, it is respectfully submitted that Applicant's Admissions do not show that the test mode circuit outputs a test mode signal according to a predetermined voltage to a predetermined terminal of a plurality of address input terminals. Additionally, it is respectfully submitted that Applicant's Admitted Prior Art fails to disclose or suggest providing a monitor terminal for confirming a test mode of the memory device from the outside. Thus, it is respectfully submitted that Applicant's Admitted Prior Art is significantly different from that of the present invention. Moreover, it is respectfully

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submitted that neither the teachings of McGibney et al. or McClure et al. overcome such shortcomings.

Specifically, it is noted that McGibney et al. merely shows a control circuit CTRL receiving an initiation signal GO to control a stress test. McGibney et al. clearly fails to show that the test mode circuit outputs a test mode signal according to a predetermined voltage supplied to a predetermined terminal of a plurality of address input terminals. Further, McGibney et al. fails to disclose or suggest a monitor terminal for confirming the test mode of the memory device from the outside.

Similarly, McClure et al. merely discloses that the burn-in test mode circuit 10 is controlled by ETD pulse which is triggered by a change in state of an address pin. However, McClure et al. clearly fails to disclose or suggest that the test mode circuit outputs a test mode signal according to a predetermined voltage to a predetermined terminal and a plurality of address input terminals. Further, McClure et al. fails to disclose or suggest a monitor terminal for confirming a test mode of the memory device from the outside. Consequently, this reference likewise fails to disclose that which is presently set forth by Applicant's claimed invention.

Therefore, in that neither the references relied on by the Examiner nor that of Applicant's Admissions disclose or suggest that the test mode circuit outputs a test mode signal according to a predetermined voltage to a predetermined terminal in a plurality of address input terminals, nor do any of the references disclose or suggest that the monitor terminal is provided for confirming a test mode of the memory device from the outside, it is respectfully submitted that Applicant's claimed invention as set forth in each of independent claims 1, 21 and 26 as well as those claims which depend therefrom clearly distinguish over the combination proposed by the Examiner and are in proper condition for allowance.

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Turning now to page 9 of the Office Action, claims 2, 22 and 27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's Admissions in view of McGibney and McClure as applied to claims 1, 21 and 26 and further in view of teachings of U.S. Patent No. 5,982,677 issued to Fontana et al. This rejection is likewise respectfully traversed in that the patent to Fontana et al. fails to overcome the aforementioned shortcomings associated with the combination proposed by the Examiner.

In reviewing the teachings of Fontana et al., it is noted that Fontana et al. merely discloses a structure of a regulator. That is, Fontana et al. likewise fails to disclose that the test mode circuit outputs a test mode signal according to a predetermined voltage to a predetermined terminal in a plurality of address input terminals. Further, Fontana et al. fails to disclose or suggest providing a monitor terminal for confirming a test mode of the memory device from the outside. Consequently, it is respectfully submitted that while Fontana et al. may disclose the drain voltage regulator referred to by the Examiner, this teaching clearly fails to overcome the aforementioned shortcomings associated with the combination proposed by the Examiner. Accordingly, it is respectfully submitted that Applicant's claimed invention as set forth in each of independent claims 1, 21 and 26 as well as those claims which depend therefrom clearly distinguish over the combination proposed by the Examiner and is in proper condition for allowance.

With reference to the Examiner's response to Applicant's arguments, set forth in paragraph 11 of the Office Action and particularly page 8 thereof, as set forth hereinabove, it is respectfully submitted that McClure et al. merely shows that the burn-in test mode circuit 10 is controlled by an ETD pulse which is triggered by a change in state of an address pin. It is respectfully submitted that this reference fails to disclose that the test mode circuit outputs a test mode signal according to a predetermined voltage to a predetermined terminal of a

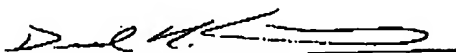
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plurality of address input terminals. That is, the test mode circuit of McClure et al. is controlled even if the predetermined test pin is not changed or even if the predetermined test pin changes and the predetermined voltage is not changed. Consequently, it is respectfully submitted that Applicant's claimed invention as set forth in each of independent claims 1, 26 and 29 clearly distinguish over the combination proposed by the Examiner including the teachings of McClure et al. Further, it is noted that McClure et al. like the other references of record fails to disclose a monitor terminal connected to the test mode circuit and outputting the test mode signal for confirming a test mode as is specifically recited by Applicant's claimed invention. Accordingly, it is respectfully submitted that Applicant's claimed invention clearly distinguishes over the combinations proposed by the Examiner and is in proper condition for allowance for at least the reasons discussed hereinabove.

Therefore, in view of the foregoing it is respectfully requested that the objections and rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-5 and 21-29 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

  
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